AAB University

Faculty of Computer Sciences

Introduction to Digital Technologies and Circuits

Week 13:

Registers and Counters

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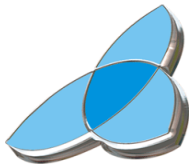
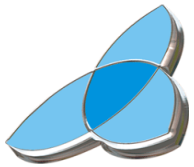
Registers and Counters



- A circuit with flip-flops is considered a sequential circuit even in the absence of combinational logic.

- Circuits that include flip-flops are usually classified by the function they perform. Two such circuits are:
  - **Registers** and
  - **Counters**

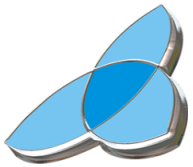
Registers and Counters



- **Register**
  - is a group of flip-flops. Its basic function is to hold information within a digital system so as to make it available to the logic units during the computing process. However, a register may also have additional capabilities associated with it.

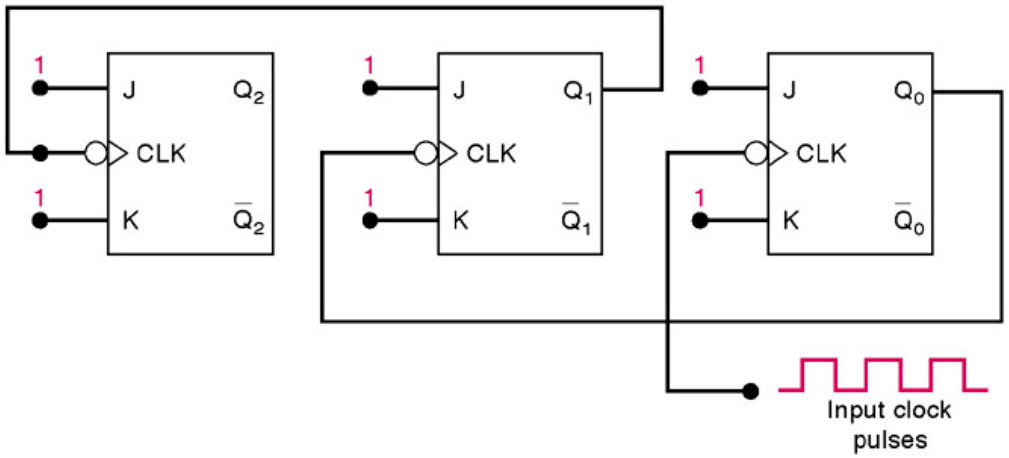
- **Counter**
  - is essentially a register that goes through a predetermined sequence of states. The gates in the counter are connected in such a way as to produce the prescribed sequence of binary states.

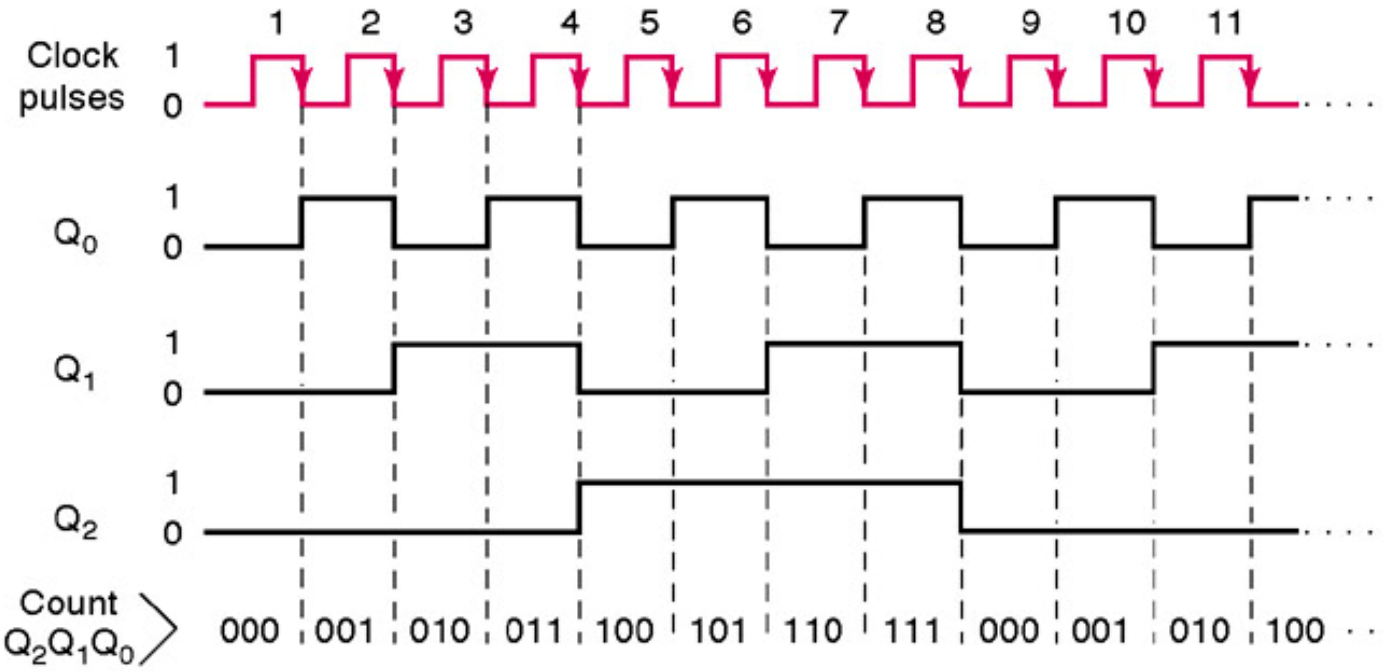
Counters



- Counters are frequently used in computers and other digital systems:
  - Event Counting,
  - Frequency Division,
  - Timing and Control Operations
- Like all other sequential logic circuits, counter circuits can be classified into two categories: asynchronous and synchronous.
  - In synchronous counters all memory elements are simultaneously triggered by a clock, whereas in asynchronous counters the output of each memory element activates the next memory element.
- Many types of counters are used in practice:
  - In some cases they count in pure binary; in other cases the count may differ considerably from straight binary (e.g., decade, BCD counters, MOD<2^N counters, est.).

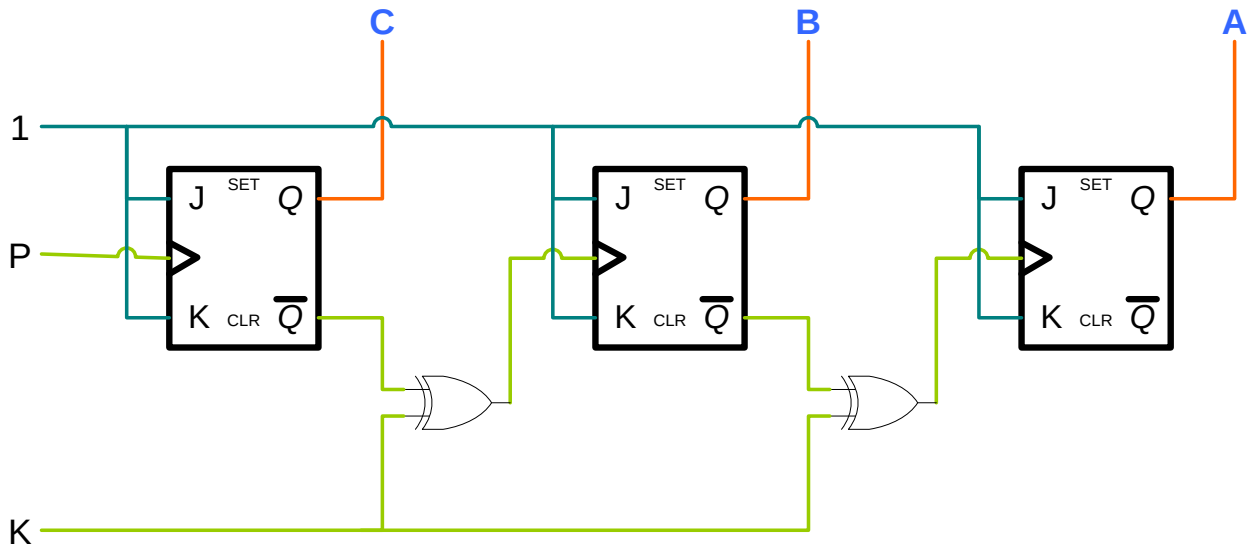
Asynchronous Counters





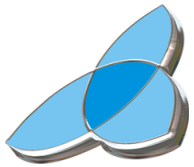
Analysis of Asynchronous Counters

- Example 1:



- Timing Diagrams…

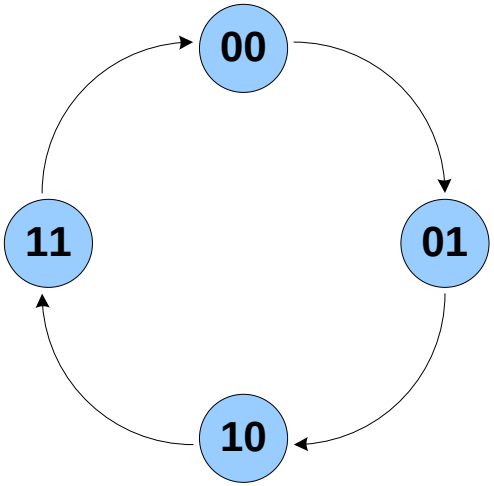
Synchronous Counters



- A synchronous counter connects all of its flip-flop clock inputs to the same common CLK signal, so that all of the flip-flop outputs change at the same time!
  - after only t_F ns of delay (t_F is the propagation delay from input to output of the flip-flop)

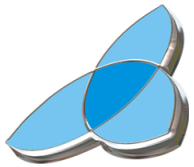
Design of Synchronous Counters

- Example 2:
  - Design a synchronous BCD counter described with the following state diagram:



  - Using:
    a) JK - Flip-Flops
    b) T - Flip-Flops
    c) D - Flip-Flops

Design of Synchronous Counters



- Example 3:
  - Design the counter with the following predetermined sequence of states:

    001 011 101 111

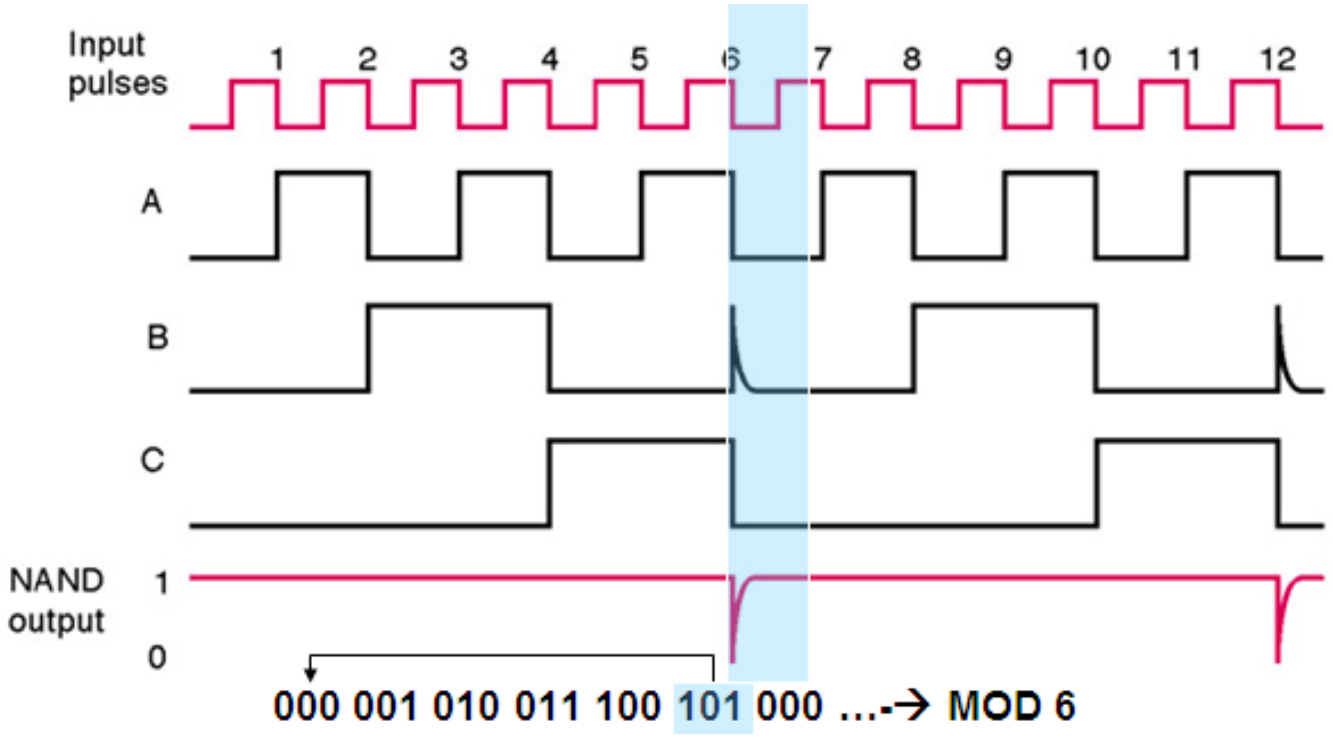
  - Increment other states to the next one!
  - Use Flip-Flops:

    a) JK - Flip-Flops
    b) T - Flip-Flops
    c) D - Flip-Flops

    and basic logic gates:

Counters with MOD < 2^N

- MOD 6 < 2^N



- Questions?!

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