AAB University

Faculty of Computer Sciences

Introduction to Digital Technologies and Circuits

Week 6, 7:

Logic Design of Combinational Circuits

Asst. Prof. Dr. **Mentor Hamiti**
mentor.hamiti@universitetiaab.com

Last Time

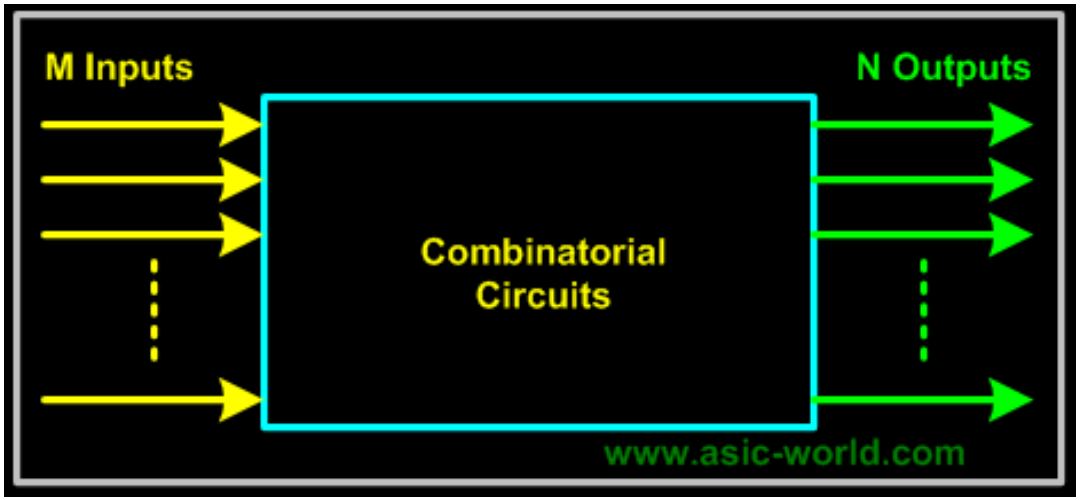
- Minimization of Logic Functions
- Combinational Logic Circuits
- Logic Gates
  - Basic Logic Gates
  - Universal Logic Gates
  - Special (exclusive) Logic Gates

Today

- Combinational Logic Circuits
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

Combinational Logic Circuits

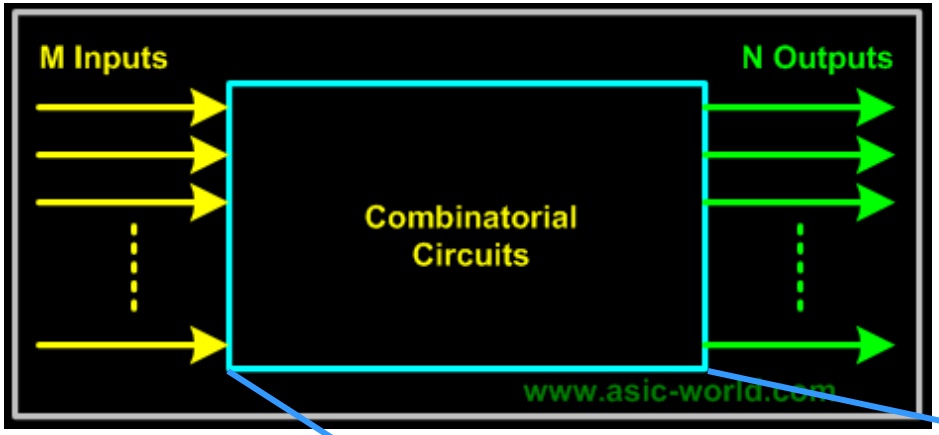
- Combinational Circuits are circuits which can be considered to have the following generic structure.



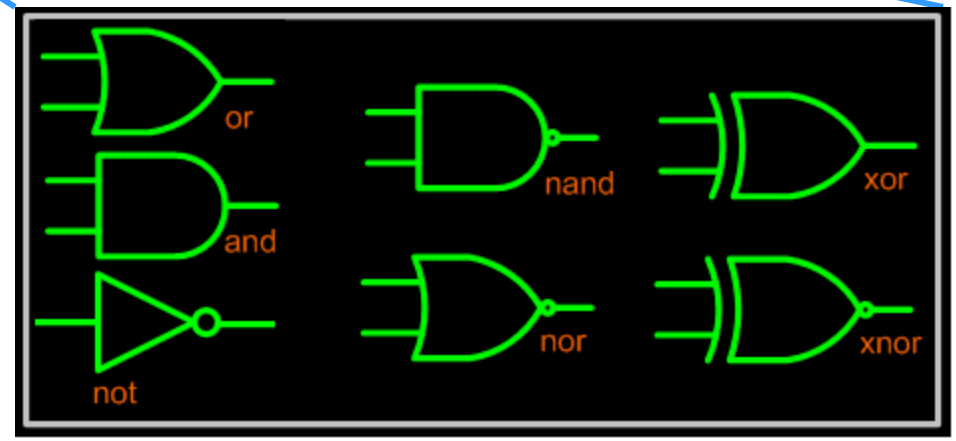
- Whenever the same set of inputs is fed in to a combinatorial circuit, the same outputs will be generated. Such circuits are said to be stateless.

Combinational Logic Circuits

- All Combinational Circuits are composed by simple combinational logic elements - "**Logic Gates**".



- Logic Gates:
  - Basic Logic Gates
  - Universal Logic Gates
  - Exclusive Logic Gates

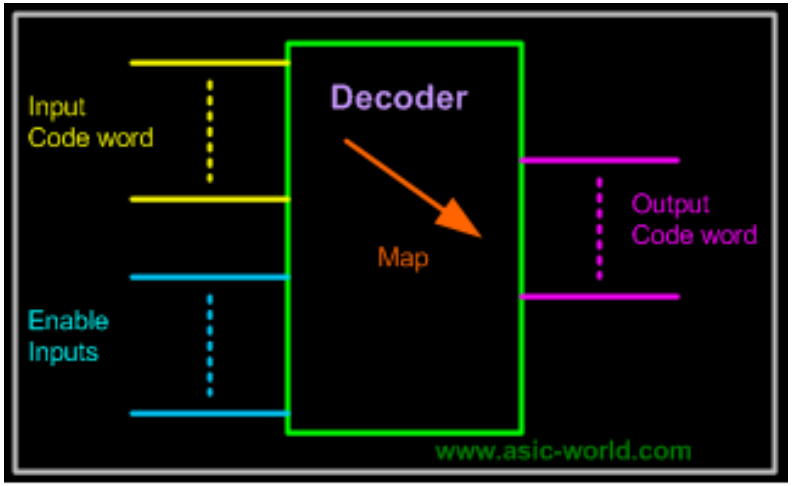


Combinational Logic Circuits

- Combinational Circuits:
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

Decoder

- A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different.
- Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding.



- Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word.

Decoder

- Binary **n-to-2^n** Decoder:

- A binary decoder has n inputs and 2^n outputs.

- **Only one output is active** at any one time, corresponding to the input value.

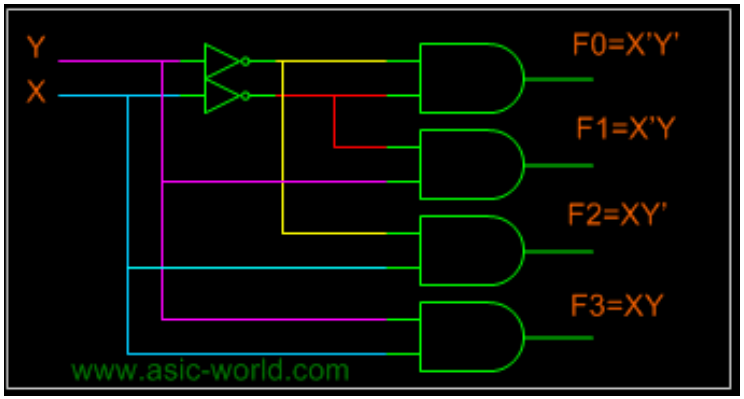
Decoder

- Binary Decoder **2-to-4**:

Truth Table:

X	Y	F_0	F_1	F_2	F_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

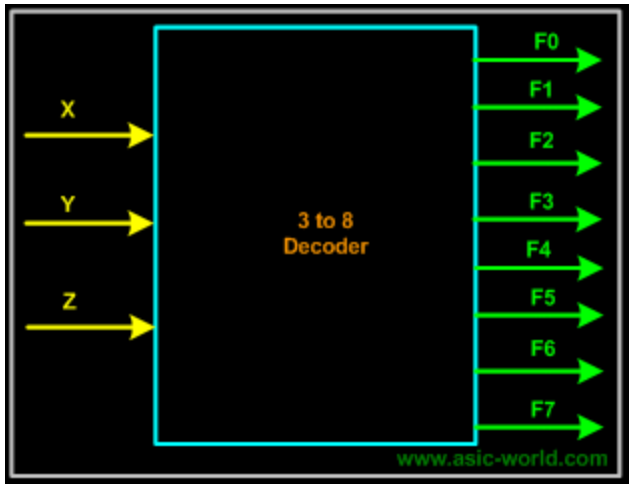
Logic Circuit:



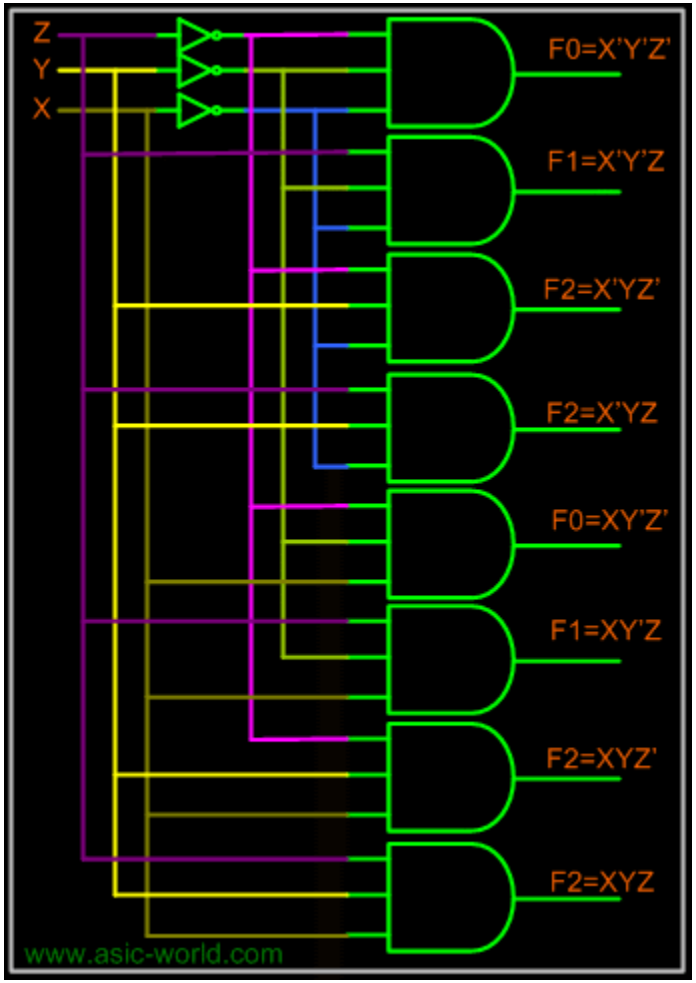
- Each output is a 2-variable minterm (X'Y', X'Y, XY', XY)

Decoder

- Binary Decoder **3-to-2^3**:



X	Y	Z	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

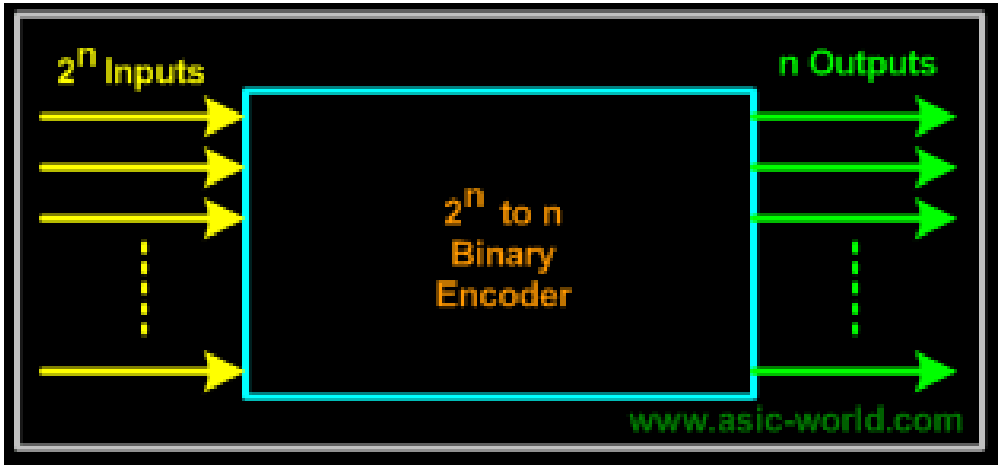


Combinational Logic Circuits

- Combinational Circuits:
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

Encoder

- An encoder is a combinational circuit that performs the inverse operation of a decoder.



- The simplest encoder is a **2^n-to-n** binary encoder, where it has only one of 2^n inputs = 1 and the output is the n-bit binary number corresponding to the active input.

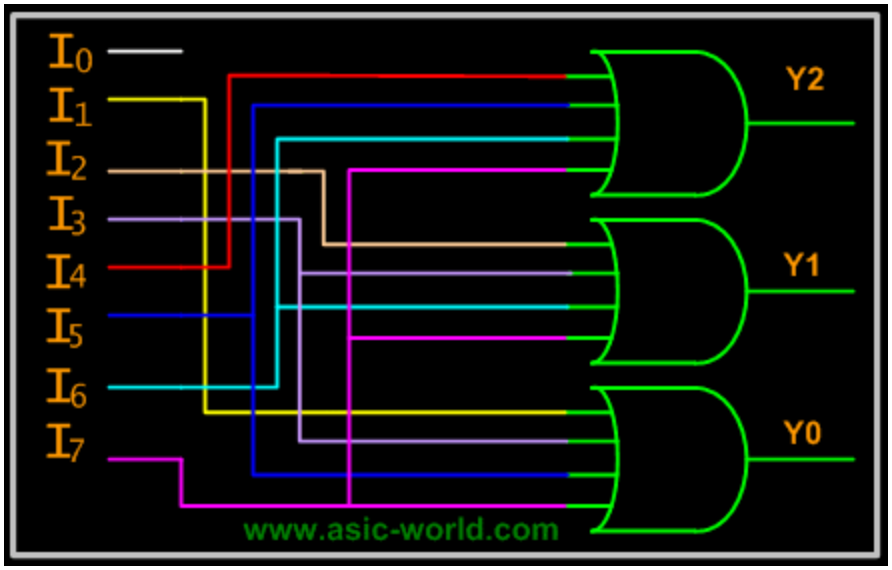
Encoder

- **Octal-to-Binary** Encoder:
- Octal-to-Binary take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1.
- The logic expressions of the outputs are: **Y0 = I1 + I3 + I5 + I7**

Y1 = I2 + I3 + I6 + I7

Y2 = I4 + I5 + I6 +I7

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



Encoder

- **Decimal-to-Binary** Encoder

- Decimal-to-Binary take 10 inputs and provides 4 outputs, thus doing the opposite of what the 4-to-10 decoder does. At any one time, only one input line has a value of 1.

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	Y_3	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

Derived functions:

$Y_3 = I_8 + I_9$

$Y_2 = I_4 + I_5 + I_6 + I_7$

$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_0 = I_1 + I_3 + I_5 + I_7 + I_9$

Priority Encoder

- If more then two inputs are active simultaneously at the Encoder circuits, the output is unpredictable or rather it is not what we expect it to be.
- This ambiguity is resolved if priority is established so that only one input is encoded, no matter how many inputs are active at a given point of time.
- The priority encoder includes a priority function. The operation of the priority encoder is such that if two or more inputs are active at the same time, the input having the highest priority will take precedence.

Priority Encoder

- Priority Encoder **4 to 3**:

- A 4 to 3 encoder consists of four inputs and three outputs. The input D3 has the highest priority, D2 has next highest priority, D0 has the lowest priority. This means output Y2 and Y1 are 0 only when none of the inputs D1, D2, D3 are high and only D0 is high.

Truth Table:

D_3	D_2	D_1	D_0	Y_2	Y_1	Y_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	x	0	1	0
0	1	x	x	0	1	1
1	x	x	x	1	0	0

Derived functions:

K-diagrams …

$Y_2 = \ldots = D_3$

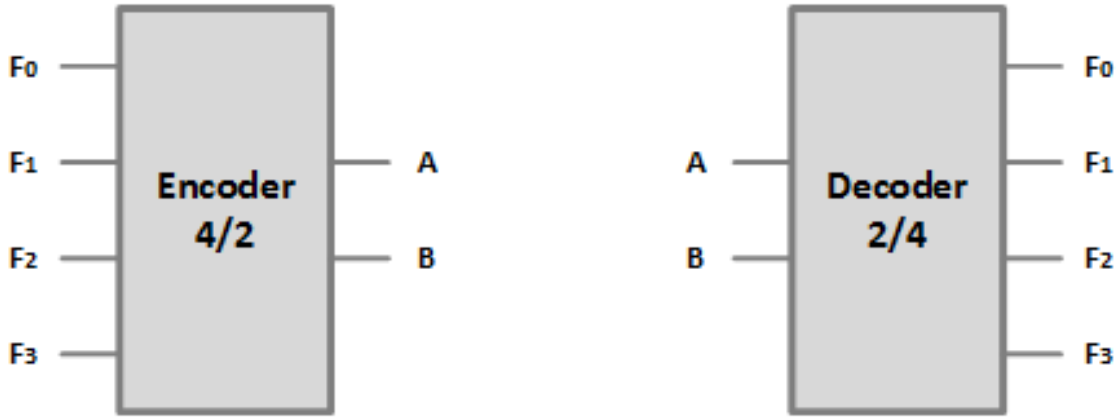
$Y_1 = \ldots = D_1 D'_3 + D_2 D'_3$

$Y_0 = \ldots = D_0 D'_1 D'_3 + D_2 D'_3$

Circuit …

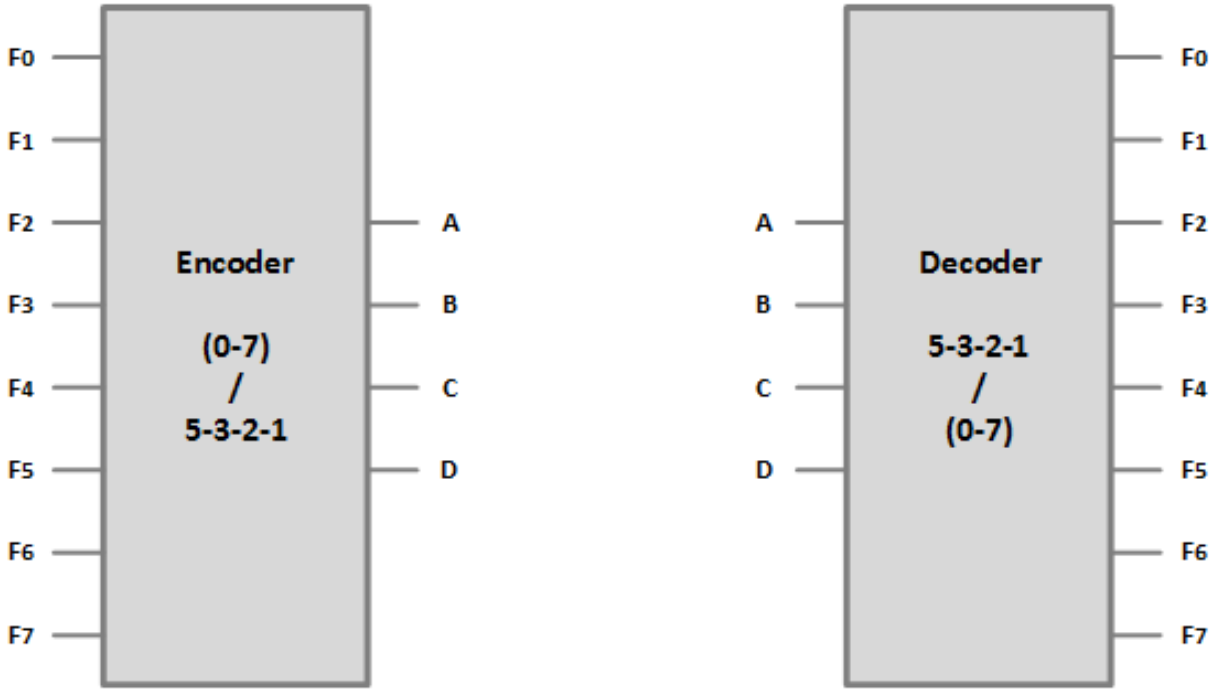
Coders and Encoders

- Example 1:
  - Design **Encoder (4/2)** and **Decoder (2/4)**, with the use of Basic Logic Gates!

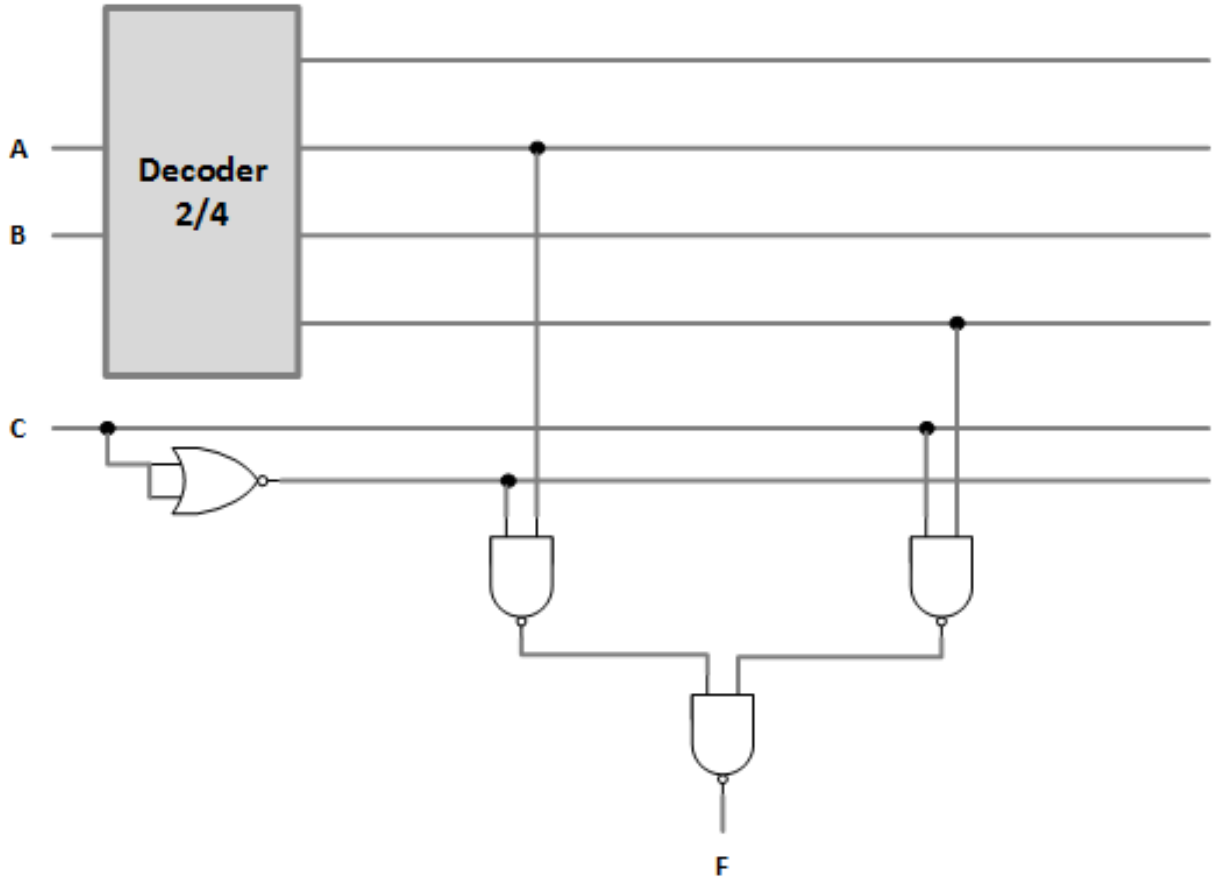


Coders and Encoders

- Example 2:
  - Construct encoder and decoder for coding and decoding **octal numbers** into and from the weighted code **5-3-2-1**.



- Example 3:
  - Find the Logic Function for the given Combinational Logic Circuit and after that design the appropriate Timing Diagram!



- Example 4:
  - If the Logic Function is given by the following Timing Diagram:

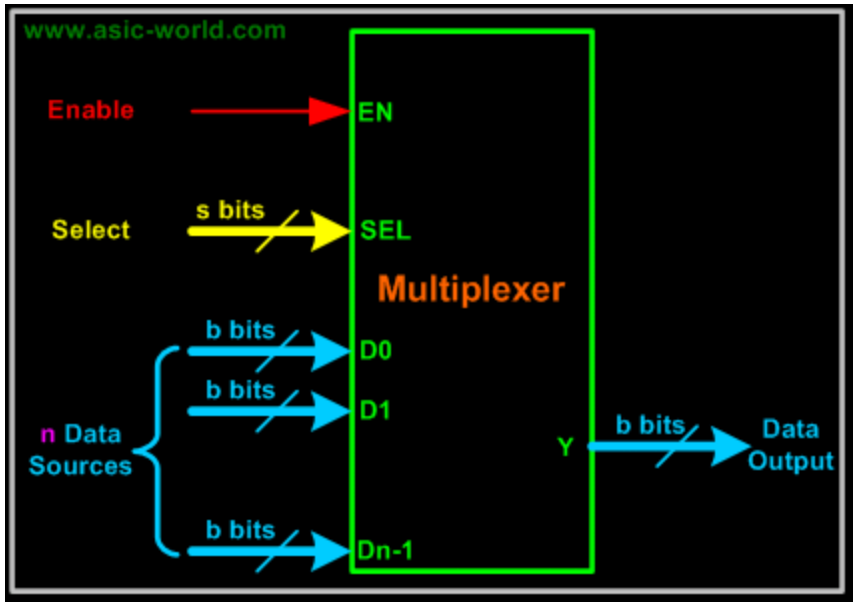
Design the Combinational Logic Circuit, with the use of two **Decoders (2/4)** and **Basic Logic Gates**!

Combinational Logic Circuits

- Combinational Circuits:
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

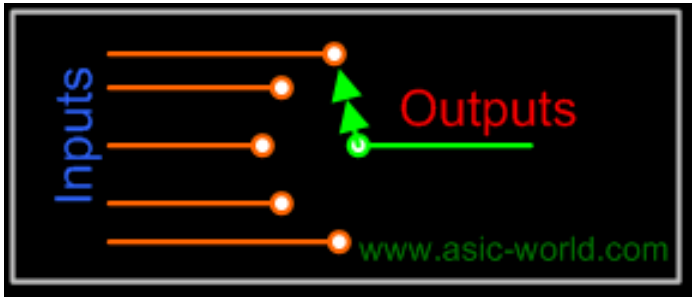
Multiplexer

- A multiplexer (**MUX**) is a digital switch which connects data from one of **n** sources to the output.
- A number of select inputs determine which data source is connected to the output.
- The block diagram of **MUX** with **n** data sources of **b** bits wide and **s** bits wide select line:

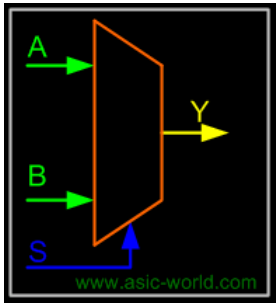


Multiplexer

- Mechanical Equivalent of a Multiplexer
- The operation of a multiplexer can be better explained using a mechanical switch as shown:



- This rotary switch can touch any of the inputs, which is connected to the output. As it is seen at any given point of time only one input gets transferred to output.
- MUX **2x1**:



S	Y
0	A
1	B

Multiplexer

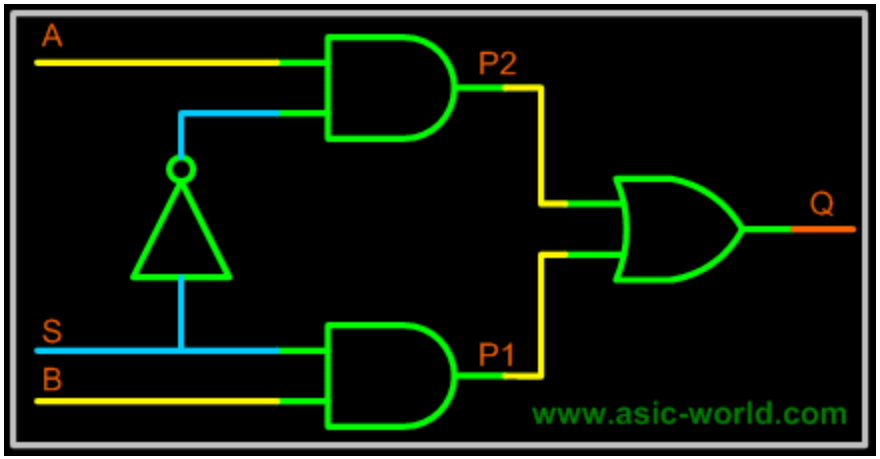
- Mux **2:1**

B	A	S	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Inputs: A, B, S

Output: $Q = A \cdot \overline{S} + B \cdot S$

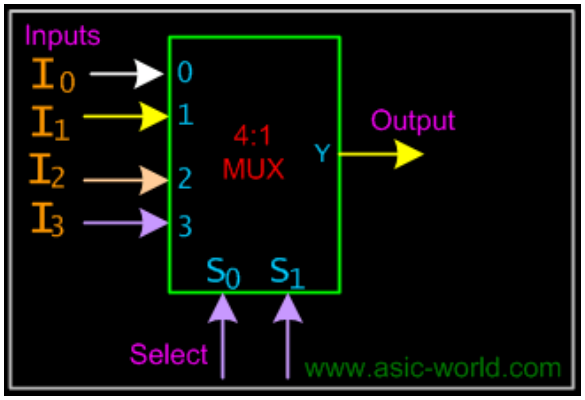
Circuit:



Multiplexer

- MUX **4:1**

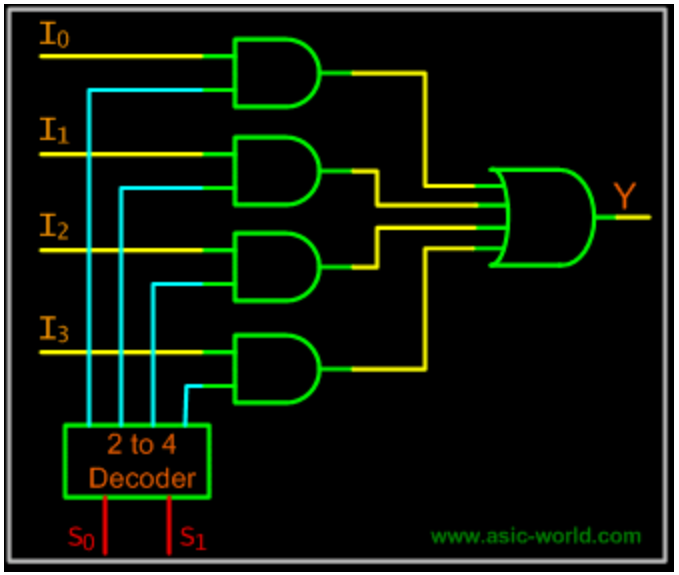
Symbol:



Truth Table

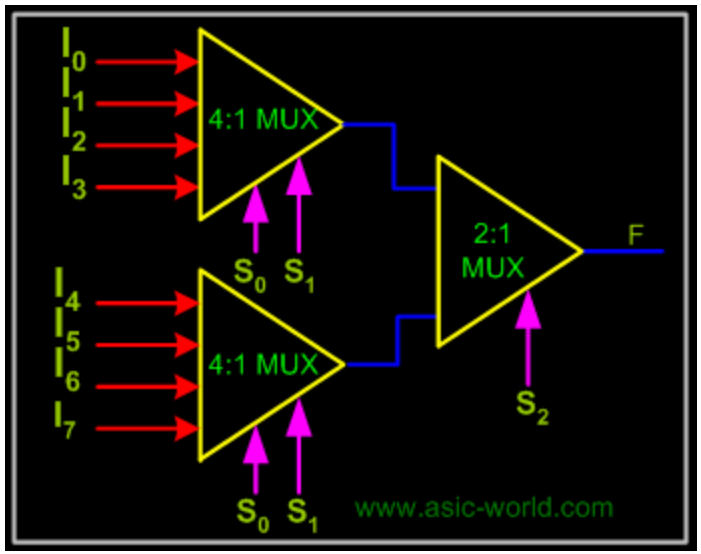
S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Circuit:

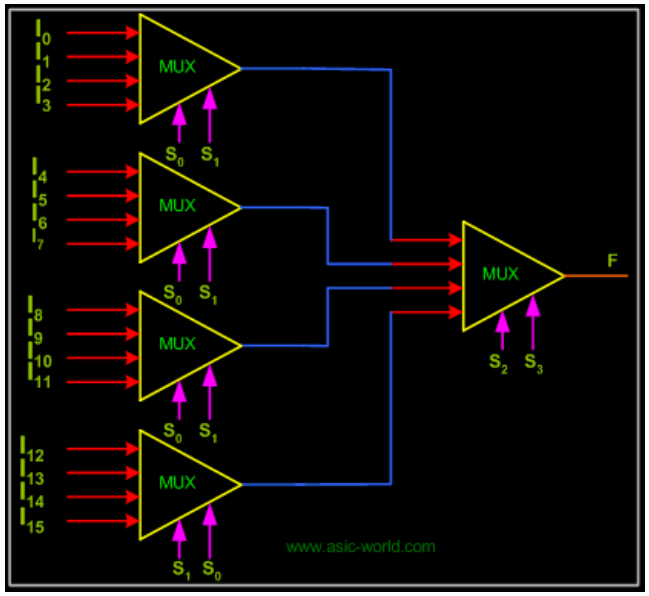


Multiplexer

- Larger Multiplexers
  - can be constructed from smaller ones.
- Example:
  - An 8-to-1 multiplexer can be constructed from smaller multiplexers.

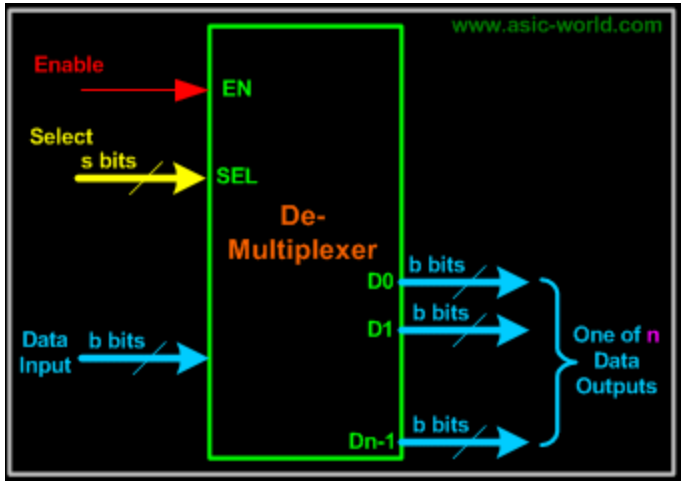


16-to-1 mux from **4:1** mux



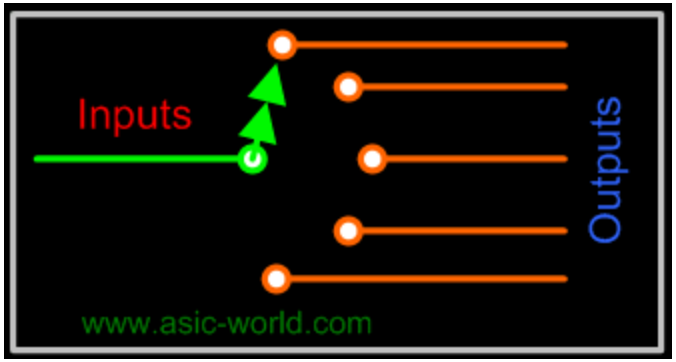
De-multiplexer

- They are digital switches which connect data from **one** input source to **one** of **n** outputs. Usually implemented by using n-to-2^n binary decoders where the decoder enable line is used for data input of the de-multiplexer.
- De-multiplexer block diagram:
  - which has got **s**-bits-wide select input, one **b**-bits-wide data input and **n** b-bits-wide outputs.



De-multiplexer

- Mechanical Equivalent of a De-multiplexer
- The operation of a de-multiplexer can be better explained using a mechanical switch as shown below:



- This rotary switch can touch any of the outputs, which is connected to the input, and at any given point of time only one output gets connected to input.

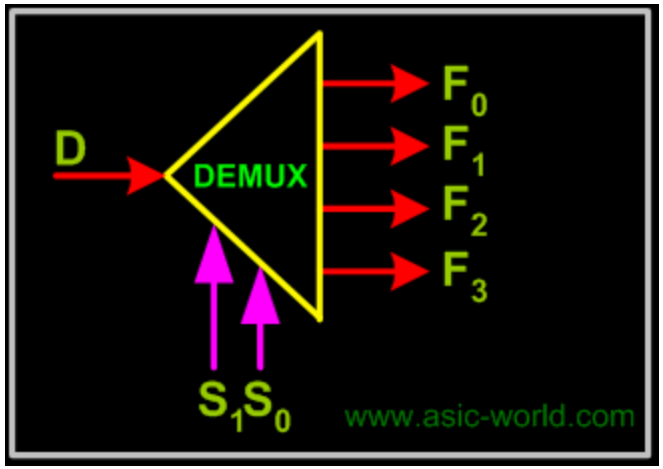
Combinational Logic Circuits

- Combinational Circuits:
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

De-multiplexer

- De-multiplexer **1-to-4**:

Symbol:

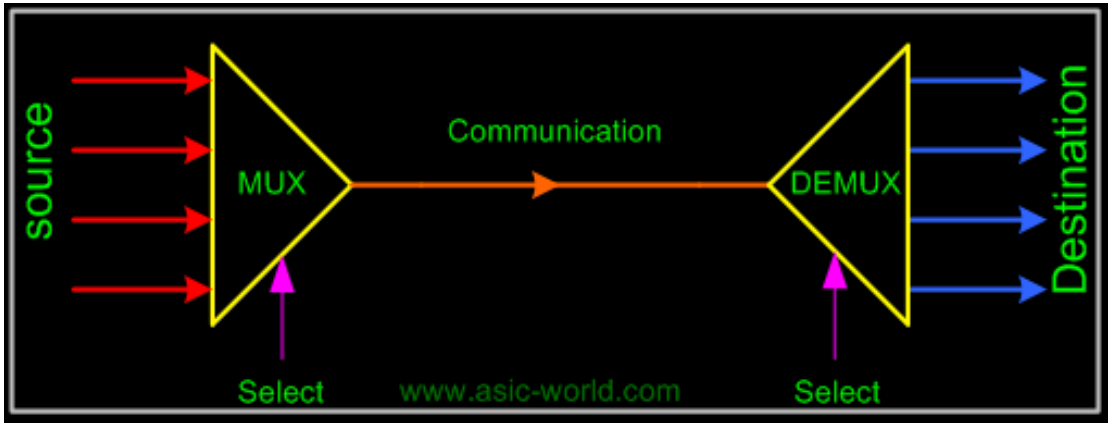


Truth table:

S_1	S_0	F_0	F_1	F_2	F_3
0	0	**D**	0	0	0
0	1	0	**D**	0	0
1	0	0	0	**D**	0
1	1	0	0	0	**D**

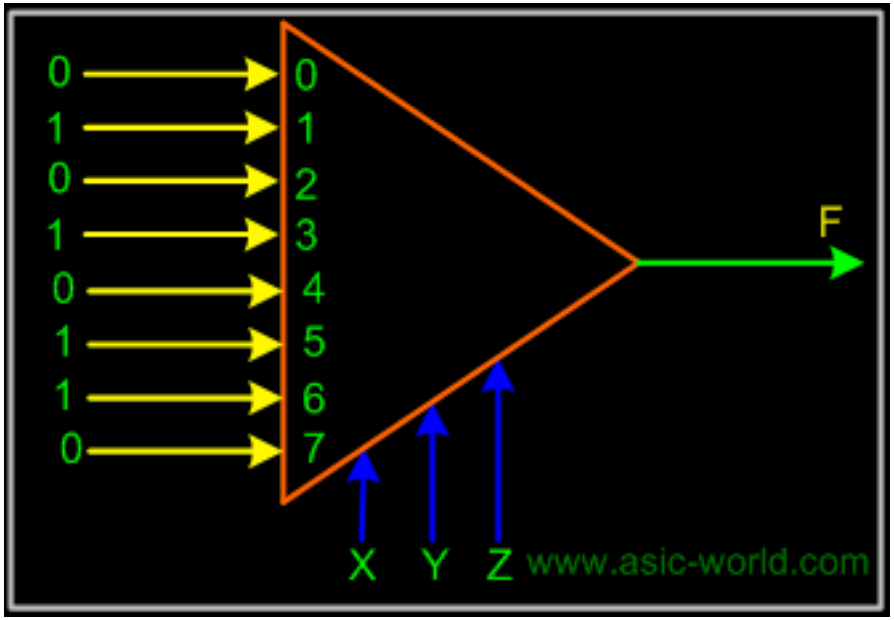
Mux-Demux Application Example

- This enables sharing a single communication line among a number of devices. At any time, only one source and one destination can use the communication line.



Multiplexers and De-multiplexers

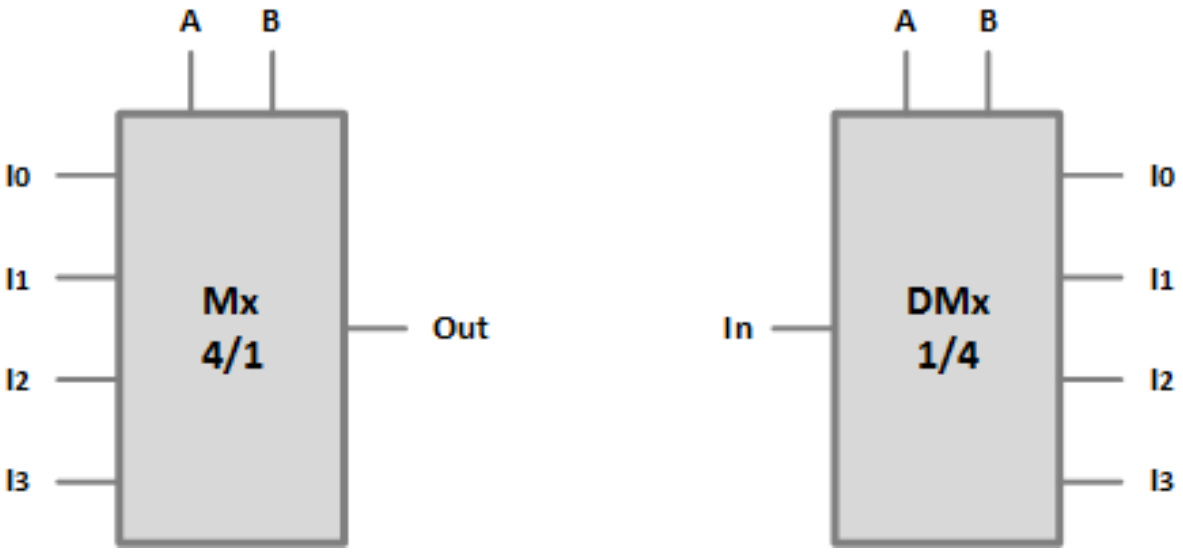
- Example 1:
  - Find the output of the following **8-to-1 multiplexer**?



$$F(X,Y,Z) = m^1(1,3,5,6)$$

Multiplexers and De-multiplexers

- Example 2:
  - Design **Multiplexer (4/1)** and **De-multiplexer (1/4)**, with the use of Basic Logic Gates!

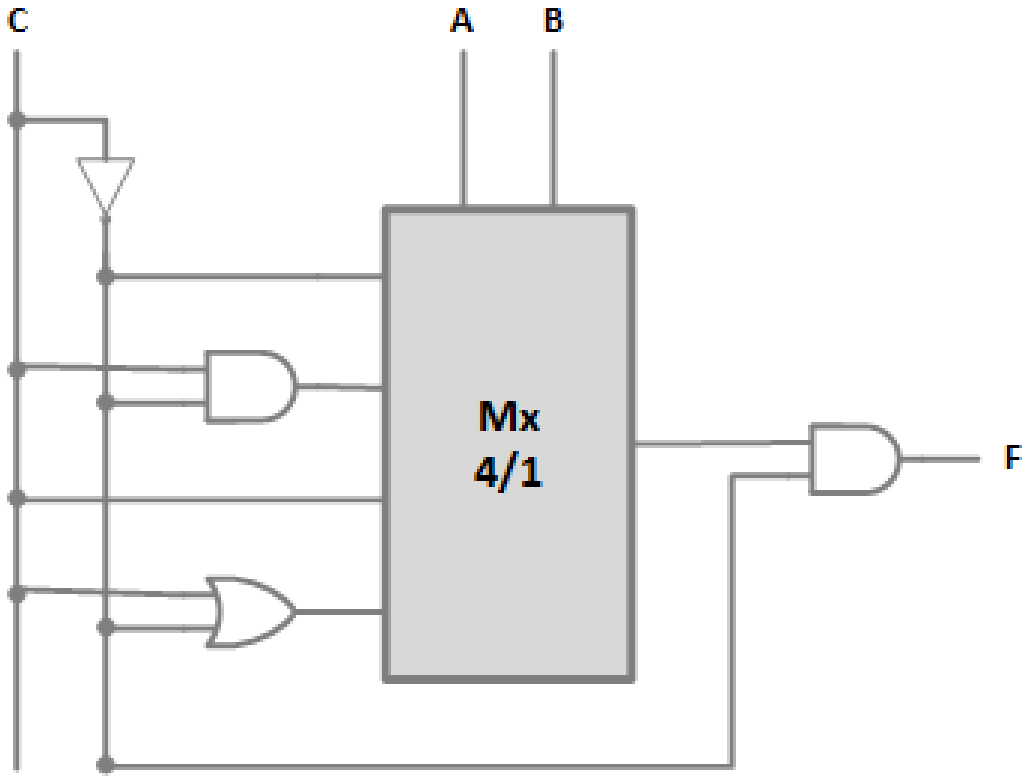


Multiplexers and De-multiplexers

- Example 3:
  - Show how **two** **4-to-1** and **one** **2-to-1 multiplexers** could be connected to form an **8-to-1 MUX** with three control inputs?!

Multiplexers and De-multiplexers

- Example 4:
  - Find the Logic Function for the given Combinational Logic Circuit and after that design the appropriate Timing Diagram and the equivalent circuit using Basic Logic Gates!

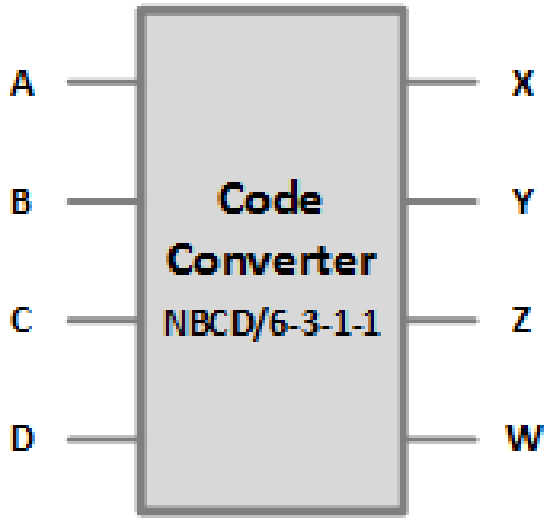


Combinational Logic Circuits

- Combinational Circuits:
  - Decoders
  - Encoders
  - Multiplexers
  - De-multiplexers
  - Other Combinational Circuits

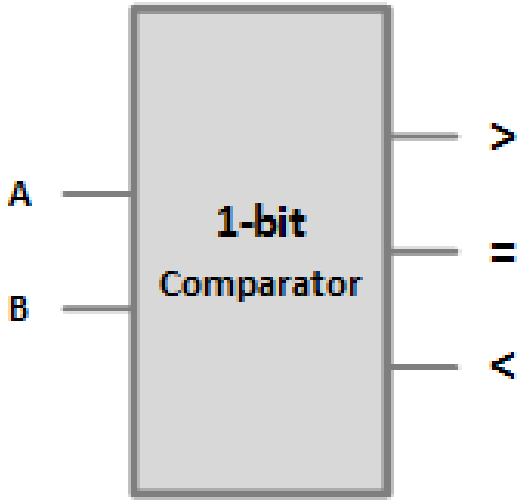
Code converters

- Example 5:
  - Design the Code converter **NBCD/6-3-1-1**



Comparators

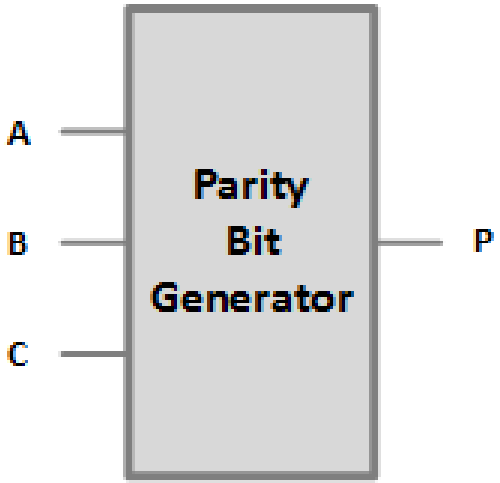
- Example 6:
  - Design the **1-bit comparator**



Parity Bit

- Example 7:
  - Design the **Parity Bit Generator** for three digits words!

A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



- Questions?!

mentor.hamiti@universitetiaab.com